## In the claims:

Please amend claims 11, 18, and 19 and cancel claims 1-10 as follows:

## 1-10. (Cancelled)

..... ... ...

11. (currently amended) A method of fabricating an electronic device comprising:

forming a film stack residing on a topmost surface of a substrate, the film stack comprising a pad oxide layer disposed on said substrate, a first nitride layer disposed on said pad oxide layer, a first polysilicon layer disposed on said first nitride layer, a second nitride layer disposed on said first polysilicon layer, and an isolation oxide layer formed on said second nitride layer;

 $\qquad \qquad \text{forming a window region by etching a portion of said} \\ \text{film stack:} \\$ 

forming a slot region for a doped polycrystalline semiconductor plug material within an outer periphery of said etched window region;

filling said slot region with said <u>doped</u> polycrystalline semiconductor plug material;

depositing a dielectric separation layer over said doped polycrystalline semiconductor plug material and on an uppermost surface of said film stack;

depositing a spacer over said dielectric separation layer;

etching said spacer and said dielectric separation layer to form a dielectric boot shape on a lower edge of said dielectric separation layer, said lower edge being a portion of said dielectric separation layer proximal to said substrate; and

redistributing a dopant from said <u>doped</u>
polycrystalline semiconductor plug <u>material</u> into said
substrate.

- 12. (original) The method of claim 11 wherein said redistributing results in a doping concentration toroidal-like in topology.
- 13. (original) The method of claim 11 further comprising implanting a dopant into an area of said substrate located in a region circumscribed by said slot region.
- 14. (original) The method of claim 11 further comprising etching through any remaining film layers within a region substantially circumscribed by said dielectric boot to said topmost surface of said substrate and depositing an emitter polycrystalline semiconductor layer over said topmost surface of said substrate.

## 15. (cancelled)

- 16. (original) The method of claim 11 wherein the spacer is comprised of oxide.
- 17. (original) The method of claim 11 wherein the spacer is comprised of polycrystalline silicon.
- 18. (currently amended) The method of claim 11 wherein the step of filling said slot region with said <u>doped</u> polycrystalline semiconductor plug material is achieved by depositing a conformal <u>doped</u> polycrystalline semiconductor plug material and anisotropically etching said <u>doped</u> polycrystalline semiconductor plug material prior to depositing a dielectric separation layer.

19. (currently amended) A method of fabricating an electronic device comprising:

forming a slot region for a doped polycrystalline semiconductor plug material within an outer periphery of an etched window region, said window region formed by etching a film stack residing on a topmost surface of a substrate;

filling said slot region with said <u>doped</u> polycrystalline semiconductor plug material;

depositing a nitride dielectric separation layer directly over said <u>doped</u> polycrystalline semiconductor plug material and on an uppermost surface of said film stack;

depositing a spacer over said dielectric separation layer;

etching said spacer and said dielectric separation layer to form a dielectric boot shape on a lower edge of said dielectric separation layer, said lower edge being a portion of said dielectric separation layer proximal to said substrate: and

redistributing a dopant from said <a href="mailto:doped">doped</a>
polycrystalline semiconductor plug <a href="mailto:mai